AF/ZZW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s):	S.-Y. Chung et al.
Case:	2-19
Serial No.:	09/765,754
Filing Date:	January 19, 2001
Group:	2634
Examiner:	Chieh M. Fan

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: /Brian Lewis/ Date: May 20, 2005

Title: Multilevel Coding with Unequal Error Protection and Time Diversity for Bandwidth Efficient Transmission

---

TRANSMITTAL OF APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are the following documents relating to the above-identified patent application:

(1) Appeal Brief; and
(2) Copy of Notice of Appeal, filed on March 17, 2005, with copy of stamped return postcard indicating receipt of Notice by PTO on March 21, 2005.

There is an additional fee of $500 due in conjunction with this submission under 37 CFR §1.17(c). Please charge **Ryan, Mason & Lewis, LLP Account No. 50-0762** the amount of $500, to cover this fee. In the event of non-payment or improper payment of a required fee, the Commissioner is authorized to charge or to credit **Deposit Account No. 50-0762** as required to correct the error. A duplicate copy of this letter is enclosed.

Respectfully submitted,

Joseph B. Ryan

Date: May 20, 2005

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

05/24/2005 EFLORES 00000036 500762 09765754
01 FC:1402 500.00 DA

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): S.-Y. Chung et al.
Case: 2-19
Serial No.: 09/765,754
Filing Date: January 19, 2001
Group: 2634
Examiner: Chieh M. Fan

I hereby certify that this paper is being deposited on this date with the U.S. Postal Service as first class mail addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Signature: _____ Date: May 20, 2005

Title: Multilevel Coding with Unequal Error Protection and Time Diversity for Bandwidth Efficient Transmission

---

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby appeal the final rejection dated November 17, 2004, of claims 1-15, 17 and 19-25 of the above-identified application.

REAL PARTY IN INTEREST

The present application is assigned to Lucent Technologies Inc., as evidenced by an assignment recorded May 1, 2001 in the U.S. Patent and Trademark Office at Reel 011775, Frame 0319. The assignee Lucent Technologies Inc. is the real party in interest.

RELATED APPEALS AND INTERFERENCES

There are no known related appeals or interferences.

STATUS OF CLAIMS

The present application was filed on January 19, 2001, with claims 1-25, and claims priority from provisional application Serial No. 60/195,506 filed April 6, 2000. Claim 16 was subsequently canceled. Claims 1-15 and 17-25 are pending in the application. Claims 1-15 and 17-25 are currently pending in the application. Claims 1, 17, 18 and 23-25 are the independent claims.

Claim 18 is allowed.

Each of claims 1-15, 17 and 19-25 stands finally rejected under 35 U.S.C. §102(b) or §103(a). Claims 1-15, 17 and 19-25 are appealed.

STATUS OF AMENDMENTS

On February 17, 2005, Applicants submitted an Amendment After Final Rejection Under 37 C.F.R. §1.116, proposing a clarifying amendment to independent claim 17 in order to address an informality objection raised by the Examiner. See the November 17, 2004 Final Office Action, at page 2, section 1. Surprisingly, the Examiner in an Advisory Action dated March 16, 2006, declined to enter the amendment, arguing that it would "raise new issues that would require further consideration and/or search." Applicants believe that the proposed amendment, responsive to a formality objection first raised in the Final Office Action, does not raise any new issues, places the application in better form for appeal, and should have been entered.

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 is directed to a method for multilevel coding of a stream of information bits in a communication system. The stream of information bits is separated into a plurality of different portions, and each of the portions is associated with one of a plurality of levels. At least one code is applied to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded. Both the coded portions of the information bits and the uncoded portions of the information bits are used to select modulation symbols for transmission in the system. Further, the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, with each class of bits comprising a plurality

of contiguous bits of the frame. Each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and the code or codes are selected so as to provide different amounts of error protection for at least a subset of the different classes of bits.

An illustrative embodiment of such an arrangement is shown in FIG. 5 of the drawings. There, it can be seen that a given frame 500 comprises four different classes of bits, namely, Class I, Class II, Class III and Class IV. Each of these different classes is a portion of the given frame 500 within the meaning of claim 1. Thus, this arrangement is an example of what is meant by the limitation of claim 1 that recites "wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits." Claim 1 also includes a limitation which recites "each class of bits comprising a plurality of contiguous bits of the frame." In the FIG. 5 arrangement, this limitation is met by the fact that the four different classes comprise uninterrupted sequential portions of the frame 500. See the specification at, for example, page 9, line 24, to page 10, line 11.

Advantageously, an arrangement of the type claimed provides significant advantages over conventional multilevel coding of the type described in the background portion of the specification, at page 2, lines 13-25. For example, the illustrative embodiment provides additional coding gain and thus improved performance in terms of bit error rate (BER) relative to conventional techniques. Further, unequal error protection and error flag generation are considerably facilitated. See the specification at, for example, page 3, line 28, to page 4, line 4.

Independent claim 17 is a method which is similar to claim 1 but specifies that the stream of information bits comprises a plurality of frames of information bits, and each of the portions of the stream of information bits comprises at least a part of a particular one of the frames, the part comprising a plurality of contiguous bits of the corresponding frame. An example is seen in the above-described illustrative embodiment of FIG. 5.

Independent claims 23 and 24 are respective apparatus and article of manufacture claims corresponding generally to claim 1. Again, an example is seen in the above-described illustrative embodiment of FIG. 5.

Independent claim 25 is a decoding method which recites operations generally complementary to those of the multilevel coding method of claim 1. In an illustrative embodiment, the method is implemented in a receiver portion 800 as shown in FIG. 8 of the drawings.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Claims 1-4, 6-8, 17, 19, 23 and 25 stand rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,323,424 (hereinafter "Fazel").

2. Claims 5 and 15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fazel in view of U.S. Patent No. 5,970,098 (hereinafter "Herzberg") and U.S. Patent No. 5,841,378 (hereinafter "Klayman").

3. Claims 9-13 and 20-22 stand rejected under §103(a) as being unpatentable over Fazel.

4. Claim 14 stands rejected under §103(a) as being unpatentable over Fazel in view of U.S. Patent No. 5,566,193 (hereinafter "Cloonan").

5. Claim 24 stands rejected under §103(a) as being unpatentable over Fazel in view of U.S. Patent No. 5,416,801 (hereinafter "Chouly").

ARGUMENT

1. §102(b) Rejection of Claims 1-4, 6-8, 17, 19, 23 and 25 over Fazel

A. Claims 1-4, 6-8, 19, 23 and 25

With regard to the §102(e) rejection, the Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §2131, specifies that a given claim is anticipated "only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference," citing Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Moreover, MPEP §2131 indicates that the cited reference must show the "identical invention . . . in as complete detail as is contained in the . . . claim," citing Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully submit that the Examiner has failed to establish anticipation of independent claims 1-4, 6-8, 19, 23 and 25 by Fazel.

As noted above, independent claim 1 calls for a particular type of multilevel coding arrangement, namely, one in which a stream of information bits that is separated into portions, with

the portions being associated with respective levels, comprises at least one frame of information bits separated into a plurality of different classes of bits, with each class of bits comprising a plurality of contiguous bits of the frame. Each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and the code or codes are selected so as to provide different amounts of error protection for at least a subset of the different classes of bits.

It is particularly important to note that the claim requires that each class of bits, corresponding to one of the levels, comprises a plurality of contiguous bits of the frame. Thus, in accordance with commonly-accepted standard definitions of the term "contiguous," each class of bits includes adjacent bits from the frame.

Referring again to the illustrative arrangement of FIG. 5, frame 500 comprises four different classes of bits, namely, Class I, Class II, Class III and Class IV. Each of these different classes is a portion of the given frame 500 within the meaning of claim 1. Thus, this arrangement is an example of what is meant by the limitation of claim 1 that recites "wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits." Furthermore, in the FIG. 5 arrangement, the four different classes comprise uninterrupted sequential portions of the frame 500. Thus, each of classes of bits in the FIG. 5 arrangement comprises a plurality of contiguous bits of the frame, as recited in the claim.

The Examiner argues that Fazel discloses each and every limitation of independent claim 1. Applicants respectfully disagree.

The Examiner particularly relies on the arrangement shown in FIG. 3 of Fazel as being allegedly anticipatory. However, it is believed that such an arrangement is nothing more than a type of conventional multilevel coding similar to that already acknowledged as prior art by Applicants in the background portion of their specification at page 2, lines 13-29. Applicants are not attempting to claim such an arrangement, and the limitations of claim 1 patentably define over such an arrangement.

In contrast to the FIG. 5 example of the claimed arrangement, the arrangement shown in FIG. 3 of Fazel does not separate a stream into portions, the portions comprising respective classes, such that each class of bits comprises a plurality of contiguous bits of the frame. Instead, what Fazel does is apply the stream 34 to a serial-to-parallel converter 30. Typically, a serial-to-parallel converter

operates on blocks of input bits of a given frame, and for a particular block supplies the bits of the block to respective ones of the converter outputs. For example, an eight-bit serial-to-parallel converter with eight outputs will typically operate on blocks of eight contiguous input bits of a given frame, one block at a time, with the first bit of the first block being supplied to the first output, the second bit of the first block to the second output, and so on. For the next block of the given frame, the process repeats, with the first bit of that block being supplied to the first output, the second bit to the second output, and so on.

As a result of this typical serial-to-parallel conversion process, none of the various outputs of the converter 30 in FIG. 3 of Fazel will comprise a plurality of contiguous bits of the given frame of stream 34. To the contrary, the m outputs of the m-bit serial-to-parallel converter 30 will receive respective ones of the m bits of each m-bit block of the given input frame, and no contiguous bits of the input frame. By way of illustration, output 1 of the converter 30 will receive bit 1, bit $m + 1$, bit $2m + 1$, and so on, none of which are contiguous bits of any frame of stream 34.

Thus, the conventional serial-to-parallel conversion process used in FIG. 3 of Fazel results in an arrangement in which the particular portions at the output of converter 30 do not contain contiguous bits of any frame of the input stream 34. The serial-to-parallel conversion process essentially "chops up" each of the m-bit input blocks of the serial input stream so that the bits of each block appear at respective ones of the m outputs, with the result that no particular converter output comprises contiguous bits of the original input frame. This is believed to constitute a direct teaching away from claim 1.

The Examiner at page 2 of the March 16, 2005 Advisory Action, in response to the foregoing argument, states that Applicants are arguing that "each of the outputs of the S/P converter 30 is only one bit." This is not what Applicants are arguing, and indicates that the Examiner has failed to understand the argument presented. What Applicants are arguing is that, given a particular frame applied to the input of converter 30, output 1 of converter 30 gets the first bit (bit 1), output 2 gets the next bit (bit 2), output 3 gets the next bit (bit 3) and so on, until the first m bits of the frame are processed, then the process starts again for the next m bits of the frame, such that output 1 gets bit $m + 1$, output 2 gets bit $m + 2$, output 3 gets bit $m + 3$, and so on. Accordingly, each output of converter 30 comprises multiple bits, but none of the multiple bits at a given output are contiguous bits of the input frame. As noted above, the multiple output bits of output 1 of converter 30 are bit

1, bit $m + 1$, bit $2m + 1$, and so on, none of which are contiguous bits of any frame of input stream 34. That is, bit 1 is not contiguous with bit $m + 1$ or bit $2m + 1$ in the given frame of the input stream. As another example, bit 1 is contiguous with bit 2 in the given frame of the input stream, but as a result of the serial-to-parallel conversion process in converter 30, bit 2 goes to another output of converter 30, namely, output 2.

Thus, Fazel fails to teach or suggest that any particular one of the m outputs of the serial-to-parallel converter 30 comprises a plurality of contiguous bits of a frame of the input data stream 34.

Since Fazel fails to teach or suggest each and every limitation of claim 1, that claim is not anticipated by Fazel.

Dependent claims 2-4, 6-8 and 19 are believed allowable at least by virtue of the dependence from claim 1.

Independent claims 23 and 25 include limitations similar to those of claim 1, and are believed allowable over Fazel for substantially the same reasons identified above with regard to claim 1.

B. Claim 17

Independent claim 17 includes separating, associating, applying and utilizing steps which are similar to those of claim 1. However, the wherein clause of claim 17 specifies that the stream of information bits comprises a plurality of frames of information bits, and each of the portions of the stream of information bits comprises at least a part of a particular one of the frames, the part comprising a plurality of contiguous bits of the corresponding frame. An example is seen in the above-described illustrative embodiment of FIG. 5. As was indicated previously, Fazel discloses an arrangement involving conventional multilevel coding, of the type disclosed by Applicants in the background portion of their specification at page 2, lines 13-29, and suffers from the same problems. The present invention as set forth in claim 17 separates a frame into portions comprising contiguous bits of that frame, as shown in the illustrative example of FIG. 5. There is no such separation of a frame into portions comprising contiguous bits of a frame in the Fazel reference. Accordingly, Fazel fails to anticipate claim 17, and fails to provide its associated advantages. Moreover, by teaching conventional multilevel coding using a serial-to-parallel conversion process to separate an input frame into portions, Fazel teaches away from the present invention as set forth in claim 17.

2. §103(a) Rejection of Claims 5 and 15 over Fazel, Herzberg and Klayman

Claims 5 and 15, which depend from independent claim 1, are believed allowable for at least the reasons identified above with regard to claim 1. The Herzberg and Klayman references fail to supplement the fundamental deficiencies of Fazel as applied to claim 1.

3. §103(a) Rejection of Claims 9-13 and 20-22 over Fazel

A. Claims 9-13 and 20

Claims 9-13 and 20, which depend from independent claim 1, are believed allowable for at least the reasons identified above with regard to claim 1.

B. Claim 21

Claim 21, which depends from independent claim 1, is believed allowable for at least the reasons identified above with regard to claim 1. This claim is also believed to define separately-patentable subject matter over Fazel, as described in greater detail below.

Dependent claim 21 specifies that in an arrangement in which there is a total of $m = 5$ levels, a lowest one of the five levels has a code rate approximately in a range of about 0.2 to 0.3, the next highest one of the levels has a code rate approximately in a range of about 0.8 to 0.9, and the next highest one of the levels has a code rate greater than about 0.9.

The Examiner argues that such an arrangement is "just a matter of design choice" and hence obvious in view of Fazel. Applicants disagree. Applicants alone have determined that the particular five-level coding arrangement set forth in the claim may be advantageous in certain applications, such as those involving IBOC-DAB systems. There is no teaching or suggestion whatsoever in Fazel regarding this particular level and coding arrangement, nor is there any indication that such an arrangement may be more advantageous than another arrangement.

C. Claim 22

Claim 22, which depends from independent claim 1, is believed allowable for at least the reasons identified above with regard to claim 1. This claim is also believed to define separately-patentable subject matter over Fazel, as described in greater detail below.

Dependent claim 22 specifies that, in an arrangement in which there is a total of $m = 4$ levels,

a lowest one of the four levels has a code rate approximately in a range of about 0.2 to 0.3, and the next two highest levels have code rates higher than about 0.9 and 0.95, respectively.

The Examiner again argues that such an arrangement is "just a matter of design choice" and hence obvious in view of Fazel. Applicants again disagree. Applicants have determined through their design efforts that the particular four-level coding arrangement set forth in the claim may be advantageous in certain applications, such as those involving IBOC-DAB systems. There is no teaching or suggestion whatsoever in Fazel regarding this particular level and coding arrangement, nor is there any indication that such an arrangement may be more advantageous than another arrangement.

4. §103(a) Rejection of Claim 14 over Fazel and Cloonan

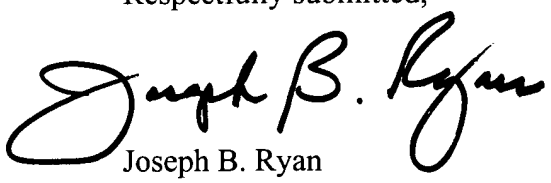
Claim 14, which depends from independent claim 1, is believed allowable for at least the reasons identified above with regard to claim 1. The Cloonan reference fails to supplement the fundamental deficiencies of Fazel as applied to claim 1.

5. §103(a) Rejection of Claim 24 over Fazel and Chouly

Independent claim 24 is believed allowable for reasons similar to those identified above with regard to claim 1. Like claim 1, independent claim 24 specifies that the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, with each class of bits comprising a plurality of contiguous bits of the frame. The claim further specifies that each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and that the at least one code is selected so as to provide different amounts of error protection for at least a subset of the different classes of bits. As was described above with reference to claim 1, Fazel fails to meet at least these limitations of claim 24. Chouly fails to supplement this fundamental deficiency of Fazel as applied to the limitations in question. Accordingly, the §103(a) rejection of claim 24 is believed to be improper, and should be withdrawn.

In view of the above, Applicants believe that claims 1-15, 17 and 19-25 are in condition for allowance, and respectfully request the withdrawal of the §102(b) and §103(a) rejections.

Respectfully submitted,



Date: May 20, 2005

Joseph B. Ryan
Attorney for Applicant(s)
Reg. No. 37,922
Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560
(516) 759-7517

CLAIMS APPENDIX

1. A method for multilevel coding of a stream of information bits in a communication system, the method comprising the steps of:

separating the stream of information bits into a plurality of different portions;

associating each of the portions of the information bits with one of a plurality of levels;

applying at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded; and

utilizing both the coded portions of the information bits and the uncoded portions of the information bits to select modulation symbols for transmission in the system;

wherein the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, each class of bits comprising a plurality of contiguous bits of the frame, and wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and wherein the at least one code is selected so as to provide different amounts of error protection for at least a subset of the different classes of bits.

2. The method of claim 1 wherein the stream of information bits comprises a stream of source-coded information bits.

3. The method of claim 1 wherein there are a total of m of the levels, and the modulation symbols are selected from a signal set of a 2^m modulation constellation.

4. The method of claim 1 wherein the at least one code comprises a block code.

5. The method of claim 1 wherein the at least one code comprises a block code concatenated with a convolutional code.

6. The method of claim 1 wherein the at least one code comprises a cyclic redundancy check (CRC) code.

7. The method of claim 1 wherein there are a total of m of the levels, arranged from a lowest level to a highest level, and the designated subset of levels includes at least the lowest level.

8. The method of claim 1 wherein there are a total of m of the levels, arranged from a lowest level to a highest level, and the designated subset includes a series of i_{max} adjacent levels beginning with the lowest level, where i_{max} is less than m.

9. The method of claim 8 wherein m is equal to five, and i_{max} is equal to four, such that there are a total of five levels, one of which is an uncoded level and four of which are coded levels.

10. The method of claim 8 wherein m is equal to five, and i_{max} is equal to three, such that

there are a total of five levels, two of which are uncoded levels and three of which are coded levels.

11. The method of claim 8 wherein m is equal to five, and i_{max} is equal to two, such that there are a total of five levels, three of which are uncoded levels and two of which are coded levels.

12. The method of claim 8 wherein m is equal to four, and i_{max} is equal to three, such that there are a total of four levels, one of which is an uncoded level and three of which are coded levels.

13. The method of claim 8 wherein m is equal to four, and i_{max} is equal to two, such that there are a total of four levels, two of which are uncoded levels and two of which are coded levels.

14. The method of claim 8 wherein the portion of the information bits for each of the levels of the designated subset has at least a block code applied thereto, and wherein rates for the block codes applied to the portions of the information bits for the series of i_{max} adjacent levels beginning with the lowest level are selected so as to have increasing code rates from a lowest code rate for the block code associated with the lowest level to a highest code rate for the block code associated with the highest of the levels in the series of i_{max} adjacent levels.

15. The method of claim 8 wherein each of a plurality of lowest levels $j = 1, \ldots j_{max}$ includes a block code concatenated with a convolutional code, where j_{max} is greater than or equal to one but less than or equal to i_{max}.

16. (Canceled)

17. A method for multilevel coding of a stream of information bits in a communication system, the method comprising the steps of:

separating the stream of information bits into a plurality of different portions;

associating each of the portions of the information bits with one of a plurality of levels;

applying at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded; and

utilizing both the coded portions of the information bits and the uncoded portions of the information bits to select modulation symbols for transmission in the system;

wherein the stream of information bits comprises a plurality of frames of information bits, and each of the portions of the stream of information bits comprises at least a part of a particular one of the frames, the part comprising a plurality of contiguous bits of the corresponding frame.

18. A method for multilevel coding of a stream of information bits in a communication system, the method comprising the steps of:

separating the stream of information bits into a plurality of different portions;

associating each of the portions of the information bits with one of a plurality of

levels;

applying at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded; and

utilizing both the coded portions of the information bits and the uncoded portions of the information bits to select modulation symbols for transmission in the system;

wherein the stream of information bits comprises a plurality of frames of information bits, and each of the portions of the stream of information bits comprises at least a part of each of the plurality of frames, the particular part of a given one of the frames corresponding to one of the portions including a plurality of contiguous bits of the given frame associated with a class of bits to be provided with a designated amount of error protection.

19. The method of claim 1 further including the step of decoding received versions of the selected modulation symbols in a multilevel decoder.

20. The method of claim 1 wherein a total code rate provided taking into account the coded portions and the uncoded portions of the information bits is approximately 0.8.

21. The method of claim 1 wherein there are a total of $m = 5$ levels, and a lowest one of the five levels has a code rate approximately in a range of about 0.2 to 0.3, the next highest one of the levels has a code rate approximately in a range of about 0.8 to 0.9, and the next highest one of the

levels has a code rate greater than about 0.9.

22. The method of claim 1 wherein there are a total of $m = 4$ levels, and a lowest one of the four levels has a code rate approximately in a range of about 0.2 to 0.3, and the next two highest levels have code rates higher than about 0.9 and 0.95, respectively.

23. An apparatus for multilevel coding of a stream of information bits in a communication system, the apparatus comprising:

an multilevel encoder receiving a stream of information bits separated into a plurality of different portions, each of the portions of the information bits being associated with one of a plurality of levels, the encoder being operative to apply at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded; and

a modulator having an input coupled to an output of the multilevel encoder, the modulator utilizing both the coded portions of the information bits and the uncoded portions of the information bits to select modulation symbols for transmission in the system;

wherein the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, each class of bits comprising a plurality of contiguous bits of the frame, and wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and wherein the at least one code is selected so as to provide different amounts of error protection for

at least a subset of the different classes of bits.

24. An article of manufacture for storing software for use in multilevel coding of a stream of information bits in a communication system, the stream of information bits being separated into a plurality of different portions, each of the portions of the information bits being associated with one of a plurality of levels, wherein the software when executed implements the steps of:

applying at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded;

utilizing both the coded portions of the information bits and the uncoded portions of the information bits to select modulation symbols for transmission in the system;

wherein the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, each class of bits comprising a plurality of contiguous bits of the frame, and wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and wherein the at least one code is selected so as to provide different amounts of error protection for at least a subset of the different classes of bits.

25. A method for decoding of a multilevel coded stream of information bits in a communication system, the multilevel coded stream of information bits being coded by separating the stream of information bits into a plurality of different portions, associating each of the portions

of the information bits with one of a plurality of levels, and applying at least one code to the portion of the information bits of each level in a designated subset of the plurality of levels, such that the portions of the information bits for one or more levels in the designated subset are coded while the portions of the information bits for one or more levels not in the designated subset are uncoded, the method comprising the steps of:

demodulating received versions of the modulation symbols to obtain outputs corresponding to each of the plurality of levels; and

decoding each of the outputs associated with a given level in the designated subset so as to obtain a received version of the corresponding portion of the information bits;

wherein the stream of information bits comprises at least one frame of information bits separated into a plurality of different classes of bits, each class of bits comprising a plurality of contiguous bits of the frame, and wherein each of the portions of the stream of information bits comprises a corresponding one of the different classes of bits within the at least one frame, and wherein the at least one code is selected so as to provide different amounts of error protection for at least a subset of the different classes of bits.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None

PTO/SB/31 (09-04)
Approved for use through 07/31/2006. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Docket Number (Optional): Chung 2-19

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)]
on March 17, 2005
Signature Lisa L. Vulpis
Typed or printed name Lisa L. Vulpis

In re Application of: S-Y. Chung et al.

Application Number	Filed
09/765,754	January 19, 2001

For: Multilevel Coding with Unequal Error Protection and Time Diversity for Bandwidth Efficient Transmission

Art Unit	Examiner
2634	Chieh M. Fan

Applicant hereby **appeals** to the Board of Patent Appeals and Interferences from the last decision of the examiner.

The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) $ 500.00

☐ Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is: $ _____

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.

☑ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. _____ . I have enclosed a duplicate copy of this sheet.

☑ A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant/inventor.

☐ assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)

☑ attorney or agent of record. Registration number 37,922

☐ attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____

Joseph B. Ryan
Signature
Joseph B. Ryan
Typed or printed name
516-759-7517
Telephone number
March 17, 2005
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of _____ forms are submitted.

Receipt in the USPTO is hereby acknowledged of:

Notice of Appeal - (Orig. & 1 copy)
Petition for Extension of Time Under
37 C.F.R. §1.136(a) - (Orig. & 1 copy)

March 17, 2005
Chung 2-19
Serial No. 09/765,754
1200-466